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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Aveek Sarkar et al.

Title: METHOD AND SOFTWARE FOR IMPROVED CIRCUIT PATH TIMING PREDICTIONS, AND CIRCUIT DESIGN PRODUCED THEREWITH

Application No.: 10/651,113 Filed: August 28, 2003

Examiner: (Unassigned) Group Art Unit: 2858

Atty. Docket No.: 004-8907 Confirmation No.: 7868

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September 19, 2005

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**37 C.F.R. § 1.97(b)**

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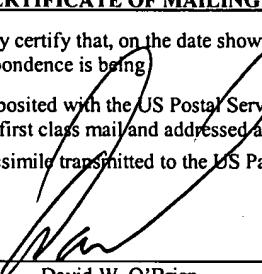
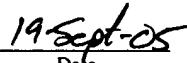
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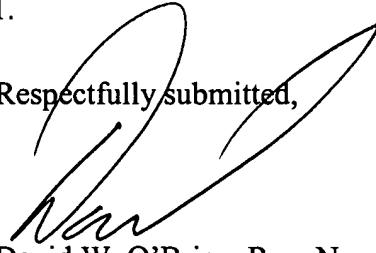
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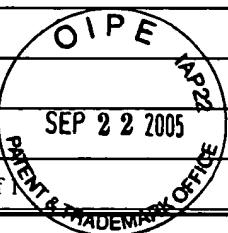
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Respectfully submitted,

  
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PTO/SB/08B (Substitute for form 1449/PTO)		Attorney Docket No.: 004-8907	
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT		First Named Inventor: Aveek Sarkar et al.	
 Sheet 1 of 1		Filing Date: August 28, 2003	
		Group Art Unit: 2858	
		Examiner Name: (Unassigned)	
		Date Submitted: September 19, 2005	
NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. <sup>1</sup>	Include name of author (in CAPITAL LETTERS), title of article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
		“Synopsys and Texas Instruments”, product description , 6 pages, Synopsys, Inc., copyright 1999.	
		Yalcin, et al. “An Advanced Timing Characterization Method Using Mode Dependency”, Proceedings of the 38th Conference on Design Automation (DAC'01), pp. 657-660, June 18-22, 2001.	
		Agah, Hamid, “Physical Synthesis”, Application Note: FPGAs, from XILINX®, XAPP140, (v1.0), 3 pages, Xilinx, Inc., February 26, 2001.	
		“PathMill: Transistor-Level Static Timing Analysis ”, 3 pages, Sysnopsys Products & Solutions, Synopsys, Inc., downloaded from <a href="http://www.synopsys.com/products">http://www.synopsys.com/products</a> , on or about May 2003.	
		Bray, Jeffrey, Sr., “Verifying timing of external IP key to SoC success”, EE Times, May 28, 2002, 3 pages, downloaded from <a href="http://www.eetimes.com">http://www.eetimes.com</a> , May 14, 2003.	
		“Transistor and gate level full chip timing analysis and automatic block characterization”, product description from Dyna, 3 pages, downloaded from <a href="http://www.circuitsemantics.com">www.circuitsemantics.com</a> , May 14, 2003.	
		“PrimeTime Synopsys Static Timing Solution”, 13 pages, 07/29/99, Revision 1.9, Sysnopsys Products & Solutions, Synopsys, Inc., downloaded from <a href="http://www.synopsys.com/products">http://www.synopsys.com/products</a> on June 5, 2003.	
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